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(54) Frequency synchroniser which uses both analogue and digital control signals

(57) A synchroniser for use in a receiver which receives signals, said synchroniser. comprising means for providing a digital control signal, said control signal defining a plurality of different levels; means for controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values; and means for estimating the difference between the levels of successive ones of said control signals.

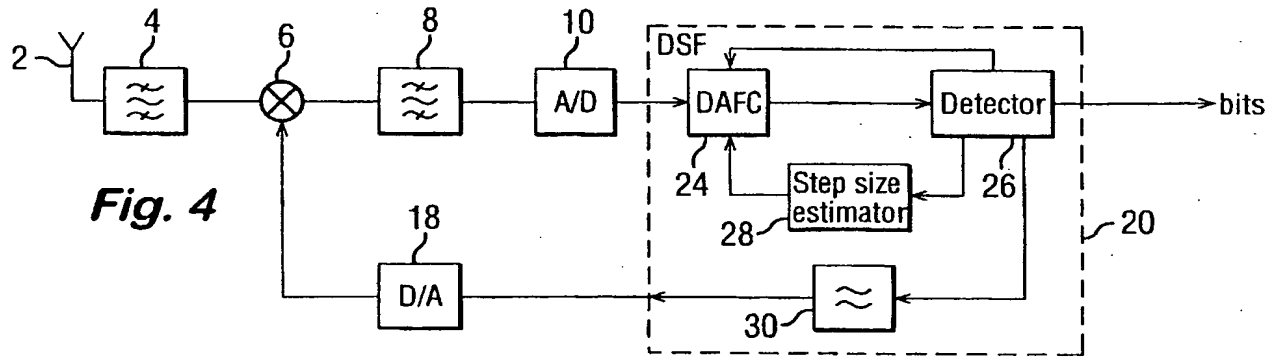

Fig. 4

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Description

[0001] The present invention relates to a synchroniser and in particular but not exclusively to a synchroniser for use in a wireless receiver in a telecommunications system.

[0002] Wireless cellular telecommunication networks are known. The area covered by the network is divided into a plurality of cells. Each cell is served by a base station which is arranged to receive signals and transmit signals to mobile stations located in the cell associated with the respective base station.

[0003] In mobile stations, the receiver is arranged to perform synchronisation with respect to the received signals. This synchronisation can be divided into two stages. Initially the signal is acquired during the acquisition phase and the initial synchronisation is performed. In the next stage, the signal is tracked. In particular, changes in the radio channel and the receiver are tracked so that synchronisation is maintained.

[0004] The following is an example of frequency synchronization. For timing, a similar arrangement can be used.

[0005] In the known receivers, this synchronisation is done for example for frequency and timing. Reference is made to Figure 2 which shows a block diagram of a known receiver. The signals are initially received by an antenna 2. The output of the antenna 2 is input to a first bandpass filter 4 which filters out the unwanted signals. Typically, the first bandpass filter 4 will allow a relatively wide range of frequencies therethrough. The output of the first bandpass filter 4 is output to a mixer 6. This mixer 6 downconverts the received radio frequency signals to a baseband frequency. This is achieved by mixing the received signal with an appropriate mixing frequency. This will be described in more detail later.

[0006] The output of the mixer 6 is input to a second bandpass filter 8 which is much narrower than the first bandpass filter. This second filter 8 is arranged to remove unwanted signals falling outside the bandwidth of the second filter. The output of the second filter 8 is input to an analogue to digital converter 10 which converts the signals from analogue to digital form. The output of the converter is output to a digital processor 12. The digital processor 12 has a detector 14 which estimates the frequency and generates a correction factor.

[0007] The correction factor is output to a third filter 16 which filters the correction value. It should be appreciated that the correction value is a digital value. The filtered corrected value is output by the digital processor 12 to a digital to analogue converter 18. The converter 12 converts the digital correction value to an analogue value. This analogue value is used to control the mixer 6 and in particular the frequency with which the output of the first bandpass filter 4 is mixed. This controls the frequency of the signals which are output by the mixer 6.

[0008] As can be seen, the synchronising elements include digital elements and analogue elements and as such are sometimes referred to as hybrid synchronisers. This can lead to problems. In particular the correction value is determined in the digital domain but the correction is done in the analogue domain. The conversion of the correction value from the digital value to the analogue value has problems associated therewith. In particular, the digital to analogue converter is not linear so the angular coefficient is not constant. Additionally, the analogue correction will suffer inaccuracies due to temperature changes, aging and operating conditions. For example the correction will vary depending on the frequency. Thus the correction made by the analogue elements will not be particularly accurate. This may mean that the variance caused by the correction is greater than the variance in the parameter estimation done in the digital processor.

[0009] A further problem is caused by the factor that the digital value is converted into an analogue value. The number of bits of the correction value provides a limitation on the accuracy of the correction. If the digital to analogue converter is able to deal with a relatively long word, it will be relatively expensive. If on the other hand the digital to analogue converter is able only to deal with relatively short words, the correction can only be done by limited step sizes. This problem is referred to as quantization noise

[0010] Reference is made to Figure 3 which shows a graph of the control value as a function the control step in a non-linear system. If this function shown in Figure 3 is well known and the minimum step is small enough, it is possible to calculate the control word so that precise control can be achieved. In practice, this is difficult to do in that this function is dependent on temperature, ageing and operating conditions. This means that even if the receiver is tuned in the factory to achieve optimum performance, this optimum performance will not be achieved once the receiver is actually used. Additionally, as mentioned previously, the minimum step size is preferred to be relatively large to minimise the costs of the digital to analogue converter.

[0011] It has been proposed to provide two loops to provide control. One loop incorporates a digital automatic frequency control which provides a fine correction. The other loop provides a rough correction. The two loops are independently controlled. The first loop is faster than the second loop. However this arrangement also has problems. The first loop can not react fast enough and hence there is a transient when second loop is controlled. For example if the rough control loop has a 500Hz step and the fine control loop has a 100Hz control loop problems arise. The first loop is unable to provide a reading if the error is greater than 100 Hz. Additionally the problem of the unknown step size means that the digital correction is not able to work correctly when the analogue control word changes. The problem is that while the frequency is estimated in the decision directed loop which requires reliable decisions, only rather small quantization steps are allowed. Otherwise the frequen-

cy error would be so large that the frequency estimation could fail in especially poor conditions and the synchroniser could become unstable.

[0012] An additional problem of acquisition is that this should be done quickly. This usually means that from time to time large corrections have to be made. This causes additional problems to those which have already been discussed

[0013] In summary, the large unknown time varying step size in the analogue correction causes a number of difficulties, as discussed above.

[0014] It is an aim of embodiments of the present invention to address one or more of the problems with the known arrangements. Embodiments of the present invention aim to provide an arrangement which provides good synchronisation even if the step size is unknown, variable and/or relatively large.

[0015] According to a first aspect of the present invention, there is provided a synchroniser for use in a receiver which receives signals, said synchroniser comprising means for providing a digital control signal, said control signal defining a plurality of different levels; means for controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values; and means for estimating the difference between the levels of successive ones of said control signals.

[0016] Thus in embodiments of the present invention, the actual analogue step size may be tracked and the remaining synchronisation error may be digitally corrected.

[0017] For a better understanding of the present invention and as to how the same may be carried into effect, reference will now be made by way of example to the accompanying drawings in which:

Figure 1 is a schematic view of a wireless cellular network in which embodiments of the present invention may be used;

Figure 2 shows a block diagram of a known receiver;

Figure 3 shows a graph of the control value as a function of the control word;

Figure 4 shows a block diagram of a processor embodying the present invention; and

Figure 5 shows a block diagram illustrating the principles of the step estimator of Figure 4.

[0018] Reference will be made to Figure 1 which shows a schematic view of a wireless cellular network in which embodiments may be used. The area covered by the network 100 is divided into a plurality of cells 102. Each cell 102 is served by a base station 104 which is arranged to transmit signals to and to receive signals from mobile stations 106 in the cell associated with the respective base station 104.

[0019] In the embodiments described, the mobile stations and the base stations use a time division multiple access technique and a frequency division multiple access technique. This means that several different frequencies are used in a network and a mobile station is allocated one of these frequencies to communicate with a base station. Likewise the base station will be allocated a frequency to communicate with the mobile station. The frequencies allocated may be the same or different. Each frequency is divided into a plurality of time slots and a mobile station will be allocated a given slot for communication, Likewise the base station will be allocated a given slot to communicate with a given mobile station. The network may be in accordance with the GSM (global system for mobile communications) standard or any other appropriate standard.

[0020] The tracking mode of embodiments of the invention will now be described. As the frequency with which the base station transmits the signals changes due to its frequency draft, jitter and so on, the mobile station needs to be able to track these changes. Additionally, the path taken by signals between the base station and the mobile station can change the frequency of the signal as it travels along that path. This effect is known as Doppler shift. Finally the mobile station has it's own frequency inaccuracies. These changes also need to be tracked.

[0021] Reference will now be made to Figure 4 which shows an embodiment of the present invention. Those elements which are the same as in Figure 2 are marked with the same reference numerals. Figure 4 shows a receiver in a mobile station.

[0022] Signals transmitted to the mobile station from the base station are received by the antenna 2. The received signals are output to a first bandpass filter 4 which has a relatively wide bandwidth. All of the signals of interest will fall in the bandwidth of the first filter 4. The filtered output is provided to a mixer 6. The filtered output is mixed with a frequency which causes the output to be at or near the base band frequency. The frequency with which the output from the first bandpass filter 4 is mixed is controlled by the output of a digital to analogue converter 18 as will be described in more detail later.

[0023] The output of the mixer 6 is input to a second bandpass filter 8. The second band pass filter has a narrower bandwidth than the first band pass filter and removes undesired signals including any undesired signals introduced by the mixer 6. The output of the second filter 8 is input to a digital signal processor DSP 20. The digital signal processor operates in a different way to that of the known receiver.

[0024] The embodiment of the present invention provides analogue control to provide a rough correction. The mixer 6 achieves this under the control of the output of the digital to analogue converter 18. Digital control for a fine correction, the frequency error and step size estimation is provided by the digital signal processor 20. The digital signal processor 20 in conjunction with the digital to analogue converter (which provides the control

signal for the analogue control, that is the mixer 6) provides a control function.

[0025] For example, when the receiver is first made, each step represents a change of 20 Hz. However, due to changes in ageing, temperature or operational conditions, each step can represent a change of more or less than 50Hz. Embodiments of the invention allow the effect of the control words to be tracked even if the frequency is changing slowly. The second band pass filter may have a tolerance of +/- 100Hz.

[0026] The digital signal processor comprises a digital automatic frequency control DAFC unit 24. The DAFC 24 is arranged to perform a more accurate correction so that a zero or as close as possible to zero error is achieved. The digital correction is controlled by a step size estimation. Thus while the control word is changed, the digital control can compensate for the effect of the analogue control for which the step size is estimated and hence known. This is the case, even if the step size changes slowly with time. The DAFC also generates the word which is used to control the digital to analogue converter.

[0027] An example of how the step estimation is used will now be described. For example the step size is 50 Hz. The analogue control is set to some value and to achieve a zero error, the digital control is set to 20 Hz in this slot. For the next slot, the analogue control is changed by one step. It is thus known that the frequency will charge by 50 Hz. Hence the digital correction must be changed to - 30 Hz to achieve a zero error. The analogue part is thus controlled for one step and due to the step size estimate, it is known by how much the frequency will be changed.

[0028] The digital automatic frequency control DAFC unit 24 has an output connected to a detector 26. The output of the detector 26 is connected to a step size estimator 28. The output of the step size estimator 28 is connected to the DAFC 24.

[0029] The step size estimator 28 is arranged to estimate the actual step size which is provided by the digital to analogue converter. This allows the effects of temperature, aging etc to be compensated. Reference will be made to Figure 5 which shows the principles used. The control word provided by the digital signal processor is changed every time slot even if it is not required. The control words selected may therefore represent the best value and the second best value. If the best value for a given time slot is the same as the best value of the previous time slot the next best value is used. If not the best value is used. In this way the effect of the step can be measured and if it changes, it can be taken into account.

[0030] Reference is made first to Figure 5a. The first level A represents the best value frequency selected as the control word to control the mixer 6. The second level B represents the second best frequency value used in the next time slot to control the mixer 6. Level C represents the actual frequency. Using two time slots, it is possible for the step size estimator to estimate the size of the step between levels A and B. In the first time slot, the step size estimator 28 estimates the step size between level A and level C. In the next time slot, the step size estimator estimates the step size between level B and level C. These two estimates are summed to give an estimate of the step size. This information is then used by the DAFC 24 when determining the fine error correction for the next time slot.

[0031] Reference is made to Figure 5b which shows the results where the step size has got smaller. As compared to the situation illustrated in Figure 5a the difference between level A and level C has decreased and the difference between level B and C has also decreased. If the step size had stayed the same, the actual frequency relative to level A would be expected at level D. Likewise if the step size had stayed the same, the actual frequency relative to level B would be expected at level E. As can be seen from Figure 5b, the level E is "higher" than level D. Using this information, it can be determined by the step size estimator that the step size has got smaller.

[0032] Reference is made to Figure 5c which shows the results where the step size has got bigger. As compared to the situation illustrated in Figure 5a the difference between level A and level C has increased and the difference between level B and C has also increased. If the step size had stayed the same, the actual frequency relative to level A would be expected at level F. Likewise if the step size had stayed the same, the actual frequency relative to level B would be expected at level G. As can be seen from Figure 5c, the level F is "higher" than level G. Using this information, it can be determined by the step size estimator that the step size has got larger.

[0033] It is assumed that the actual frequency in the examples of Figures 5b and 5c has not changed.

[0034] Reference is made to Figure 5d which shows the results where the step size has stayed the same but that the actual frequency has changed. As compared to the situation illustrated in Figure 5a the difference between level A and level H representing the actual frequency has increased and the difference between level B and level H has decreased. This means that the actual frequency of a previous slot, level C is either higher or lower than the actual frequency in the current slot. In the case of a decreasing frequency, this would result in two "positive" errors and in the case of an increasing frequency, this would result in two "negative errors". Using this information, it can be determined by the step size estimator that the step size has stayed the same and that the actual frequency has changed.

[0035] The output of the detector 26 is connected to the input of a filter 30. The detector 26 measures the frequency error. The filter 30 filters the digital word output by the detector 26. The filtered digital word is output from the digital signal processor 20 and input to the digital to analogue converter 18 which converts the digital control word into an analogue control signal which is used to control the frequency with which the input signal

is measured. As mentioned above, in each successive step, the frequency which is mixed with the received signal is also changed. The step sizes are relatively large, without the digital correction. However the step sizes are such that any desired signal will be able to pass through the second bandpass filter 8,

[0036] A correction is provided by the analogue control, that is by the mixer 6 operating under the control of the control word generated by the digital signal processor. The purpose of this correction is to ensure that the signal output by the mixer passes through the second bandpass filter.

[0037] The use of hybrid synchronisation is advantageous particular where automatic frequency control is used. The frequency of the signal output by the mixer 6 has to be controlled so that it is able to pass through the second bandpass filter 8. It should be appreciated that in alternative embodiments of the invention, other methods of control other than automatic frequency control may be used.

[0038] In summary, analogue correction is provided for a rough correction. Digital correction is provided for a fine correction. The frequency error is estimated by the detector. The actual step size used in the analogue correction is estimated by the step size estimator. The DAFC also controls the division of the correction between the analogue and digital parts. The analogue control signal is changed each slot so that the effect of one step can be measured. The digital control compensates for the effect of this known change in the frequency error while the step size estimation is valid. The step size and frequency error estimations are updated based on the frequency error changes.

[0039] Embodiments of the present invention may provided accurate synchronisation even if the step size is relatively (because the digital to analogue converter has a small word length), the step size is unknown and/or the step size is variable (linear or non linear).

[0040] The acquisition mode will now be described.

[0041] Thus, in the tracking mode, the analogue control is changed slot by slot. The frequency error is measured and the size estimation is updated. The remaining error is then removed digitally.

The acquisition mode will now be described.

[0042] The initial acquisition of the signal should be performed as quickly as possible. In hybrid systems, fast synchronisation times usually mean that large corrections need to be made from time to time. To take into account the non linearity and time variant changes, the angular coefficient of the digital to analogue converter is adaptively estimated based on two consecutive error estimates. By using two consecutive error estimates the non linearity in the digital to analogue converters can be taken into account and compensated. Using adaptive control step estimation as will described in more detail later, the synchronisation time can be decreased because the very large corrections become more accurate. In particular, the effect of temperature changes, component inaccuracies and ageing on the digital to analogue converter can be compensated. Additionally if the angular coefficients of the digital to analogue converter are tuned, these values can be updated based on the measurement using the adaptive control structure which will now be described.

[0043] The steps which are performed will now be described:

[0044] In the first step, the first adjustment is based on the fixed or tuned angular coefficient. The initial control word or correction value can be expressed as:

$$C_0 = e_0/\forall_0$$

where e_0 is the synchronisation parameter error in the first measurement and $\forall_0$ is the initial guess for the angular coefficient of the digital to analogue converter.

[0045] In the next slot n or step, a new synchronisation error e_n is calculated and a new angular coefficient $\forall_n$ is calculated.

$$\forall_n = (e_{n-1}-e_n)/C_{n-1}$$

[0046] The next control word is thus:

$$C_n = e_n/\forall_n$$

[0047] These steps are repeated until synchronisation is achieved.

[0048] In embodiments of the present invention, the fixed or tuned angular coefficient can be updated so that the next time acquisition occurs, the last estimate of the angular coefficient can be used as the initial value is the first step. In some embodiments of the invention where the digital to analogue converter is very non linear, the receiver can have a table of values for the fixed or tuned angular coefficient values for example as a function of synchronisation error. The most appropriate fixed or tuned angular coefficient value can be selected in the first stage as the initial value.

[0049] The error correction and error detection takes place in the analogue domain.

[0050] In embodiments of the present invention, the benefits of hybrid (analogue and digital) and all digital synchronisation are combined without requiring a digital to analogue converter which is capable of dealing with small sized steps. The current analogue step size is tracked and in next step, the control is calculated with the aid of estimated step size.

[0051] Thus embodiments of the present invention may be particularly advantageous when used in automatic frequency control where the frequency of the down converted signals needs to be controlled to ensure that the desired signal is passed through the second filter. The control part is thus performed before the signal

is sampled, that is converted from analogue to digital form.

[0052] Thus, in the acquisition mode, an attempt is made to control the error to be zero by the analogue circuit based on the estimated frequency error and an initial guess of the step size. The error is measured and the step estimation is updated. The control word is then calculated with the new estimate. This is continued until the error is small enough.

[0053] It should be appreciated that whilst embodiments of the present invention have been described in the context of a mobile station, embodiments of the invention may be incorporated in any suitable receiver. The receiver may be incorporated in the base station. The receiver can be used in contexts other than wireless cellular telecommunication networks and can be used wherever synchronisation is required. Embodiments of the present invention may even be used in non-wireless receivers where signals are received from a cable or the like.

[0054] In the preferred embodiment of the present invention, the synchronisation parameter which is controlled is frequency. In alternative embodiments of the invention, other parameters may be controlled such as timing, symbol synchronisation or the like.

[0055] In the embodiment shown, the down conversion to the base band frequency has been done in one step. In alternative embodiments, this down conversion make be done in two or more steps. In that case, the control provided by the digital signal processor is provided to any one of the mixers.

[0056] The preferred embodiment of the present invention has been described in the context of a frequency/ time division multiple access system. Embodiments of the present invention can be used with systems which use a frequency division multiple access system or a time division multiple access system or even a spread spectrum technique such as code division multiple access. Embodiments of the present invention may also be used with hybrids of two or more of these access techniques.

Claims

1. A synchroniser for use in a receiver which receives signals, said synchroniser comprising:

   means for providing a digital control signal, said control signal defining a plurality of different levels;
   means for controlling the level provided by successive ones of said control signals, successive ones of said control signal defining different values; and
   means for estimating the difference between the levels of successive ones of said control signals.

2. A synchroniser as claimed in claim 1 wherein said digital control signal is converted into an analogue control signal.

3. A synchroniser as claimed in claim 1 or 2, wherein said providing means, said controlling means and said estimating means are in the digital domain.

4. A synchroniser as claimed in claim 3, wherein said providing means, said controlling means and said estimating means are provided in a digital signal processor.

5. A synchroniser as claimed in any preceding claim, wherein said providing means comprises a digital corrector.

6. A synchroniser as claimed in any preceding claim, wherein a rough correction is provided by said control signal.

7. A synchroniser as claimed in claim 7, wherein said rough correction is provided in an analogue domain.

8. A synchroniser as claimed in claim 6 or 7, wherein a finer correction is provided.

9. A synchroniser as claimed in claim 8, wherein said finer correction is provided in a digital domain.

10. A synchroniser as claimed in any preceding claim, wherein said estimator is arranged to determine that the difference between two successive levels has increased if a difference between the upper of said levels and a estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

11. A synchroniser as claimed in any preceding claim, wherein said estimator is arranged to determine that the difference between two successive levels has increased if a difference between the upper of said levels and a estimated level for an actual signal provides a signal at a higher level than a signal provided by a difference between a lower of said levels and an estimated level for the actual signal.

12. A synchroniser as claimed in any preceding claim, wherein said estimator is arranged to determine that an actual signal has changed if a difference between the upper of said levels and an actual signal provides a signal at substantially the same level as a signal provided by a difference between a lower of said levels and the actual signal, said same level being different to a previous level for said actual signal.

13. A synchroniser as claimed in any preceding claim, wherein said synchroniser is arranged to acquire and/or track frequency error.

14. A synchroniser as claimed in any preceding claim, wherein said synchroniser is arranged to acquire and/or track timing error.

15. A receiver comprising a synchroniser as claimed in any preceding claim.

16. A receiver as claimed in claim 15, wherein said control signal is used to control a mixing frequency.

Fig. 1

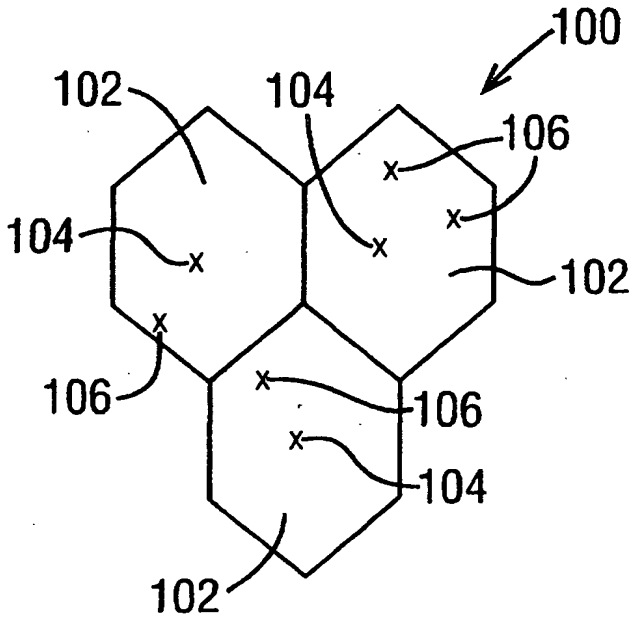
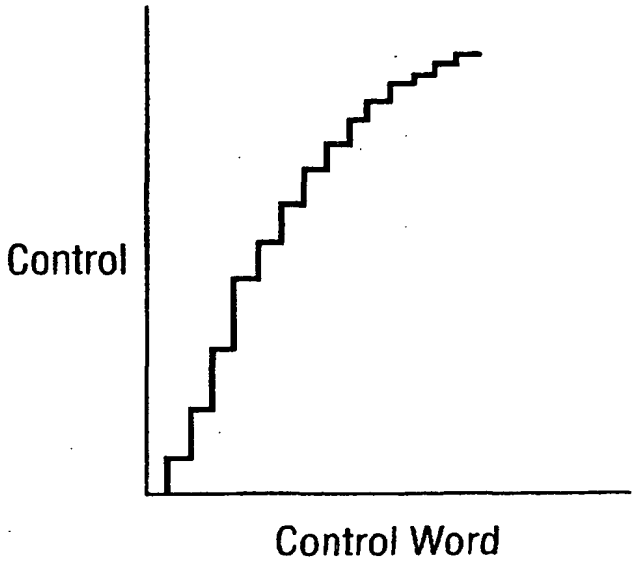
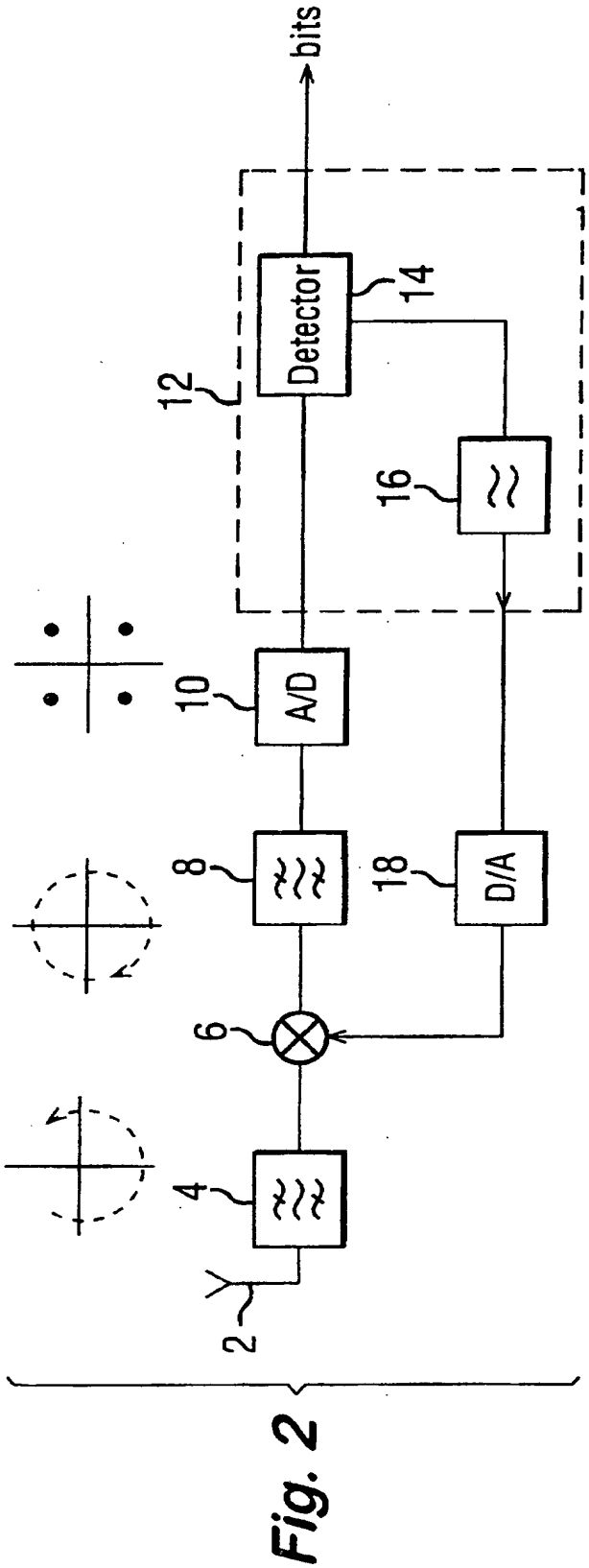


Fig. 3

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Detector
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A/D
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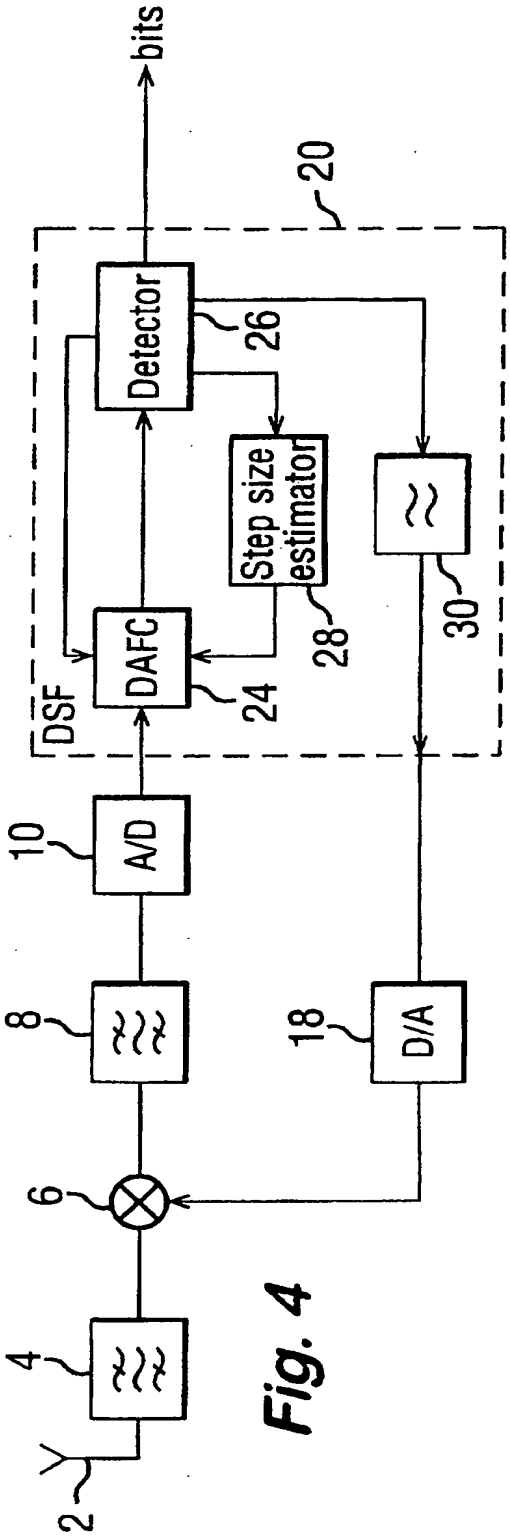
18
D/A
6
4
Y
2

Fig. 2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26
Step size estimator
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DAFC
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A/D
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18
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Y
2

Fig. 4

Fig. 5d

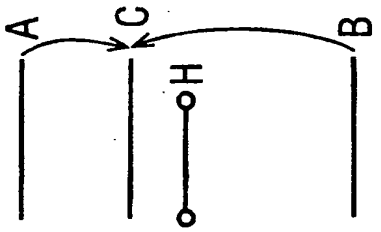

Fig. 5c

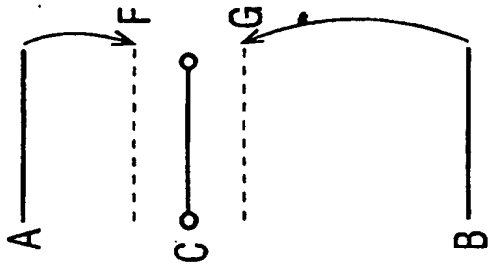

Fig. 5b

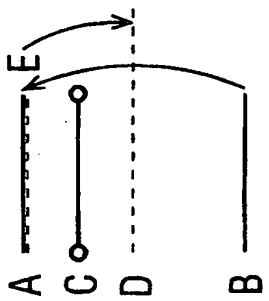
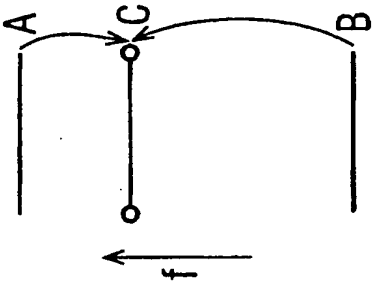
Fig. 5a